

# DATA SHEET

For a complete data sheet, please also download:

- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC

## **HEF4517B**

## **LSI**

## **Dual 64-bit static shift register**

Product specification  
File under Integrated Circuits, IC04

January 1995

# Dual 64-bit static shift register

**HEF4517B**  
**LSI**

**DESCRIPTION**

The HEF4517B consists of two identical, independent 64-bit static shift registers. Each register has separate clock (CP), data input (D), parallel input-enable/output-enable ( $PE/\overline{EO}$ ) and four 3-state outputs of the 16th, 32nd, 48th and 64th bit positions ( $O_{16}$  to  $O_{64}$ ). Data at the D input is entered into the first bit on the LOW to HIGH transition of the clock, regardless of the state of  $PE/\overline{EO}$ .

When  $PE/\overline{EO}$  is LOW the outputs are enabled and the device is in the 64-bit serial mode.

When  $PE/\overline{EO}$  is HIGH the outputs are disabled (high impedance OFF-state), the 64-bit shift register is divided into four 16-bit shift registers with D,  $O_{16}$ ,  $O_{32}$  and  $O_{48}$  as data inputs of the 1st, 17th, 33rd, and 49th bit respectively. Schmitt-trigger action in the clock input makes the circuit highly tolerant to slower clock rise and fall times.

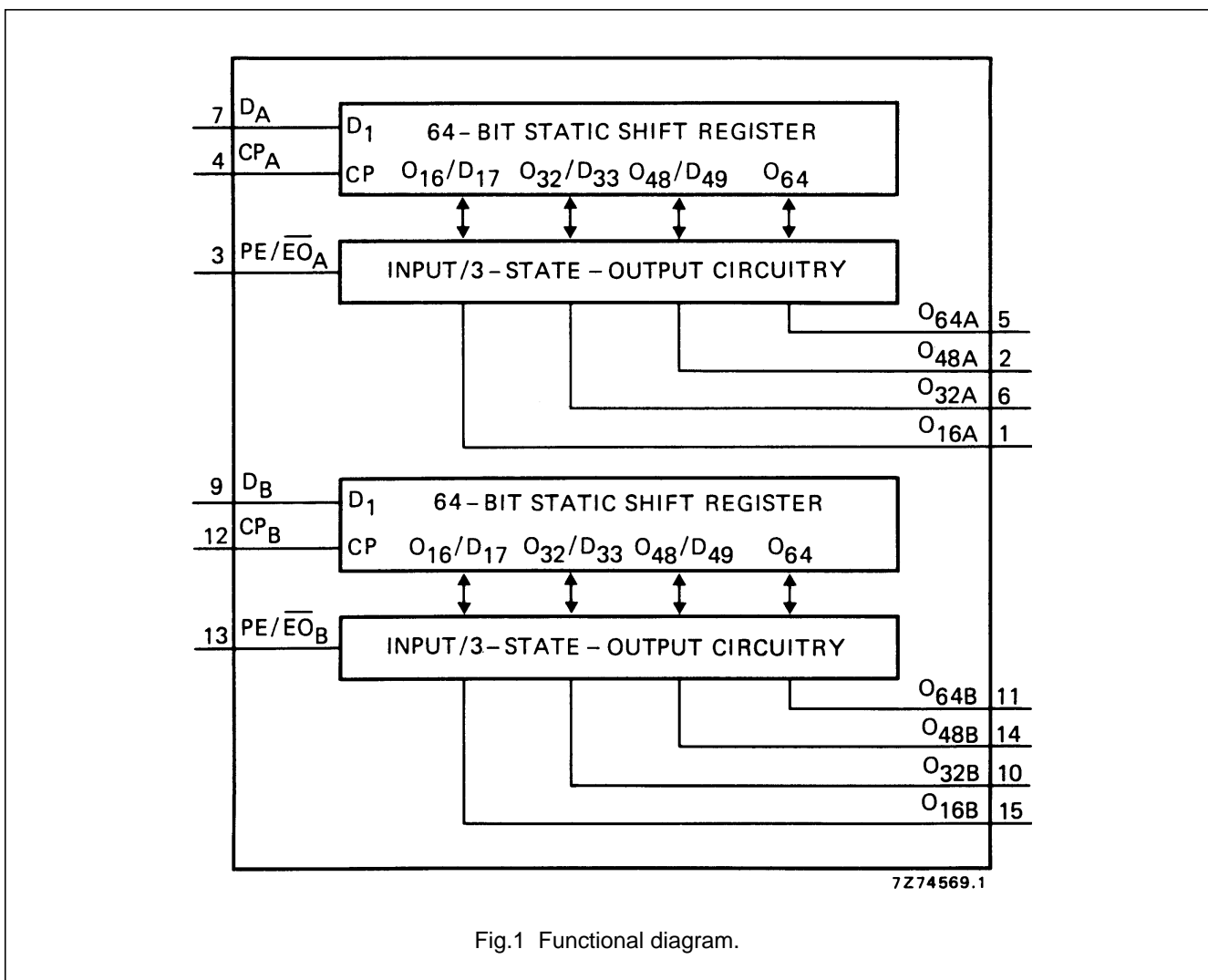


Fig.1 Functional diagram.

**FAMILY DATA, I<sub>DD</sub> LIMITS category LSI**

See Family Specifications

## Dual 64-bit static shift register

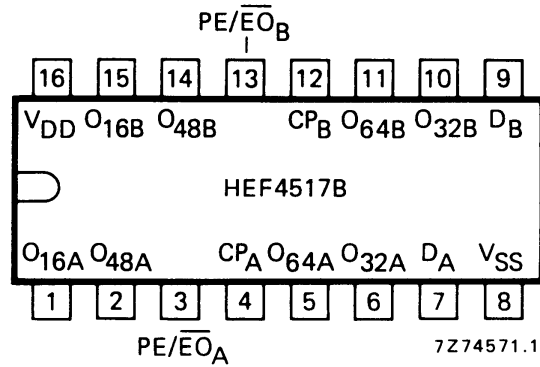
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Fig.2 Pinning diagram.

HEF4517BP(N): 16-lead DIL; plastic (SOT38-1)

HEF4517BD(F): 16-lead DIL; ceramic (cerdip) (SOT74)

HEF4517BT(D): 16-lead SO; plastic (SOT109-1)

( ): Package Designator North America

**PINNING**

$CP_A, CP_B$	clock inputs
$PE/\overline{EO}_A, PE/\overline{EO}_B$	parallel input-enable/output-enable inputs
$D_A, D_B$	data inputs
$O_{16A}, O_{32A}, O_{48A}$	3-state outputs/inputs
$O_{16B}, O_{32B}, O_{48B}$	3-state outputs/inputs
$O_{64A}, O_{64B}$	3-state outputs

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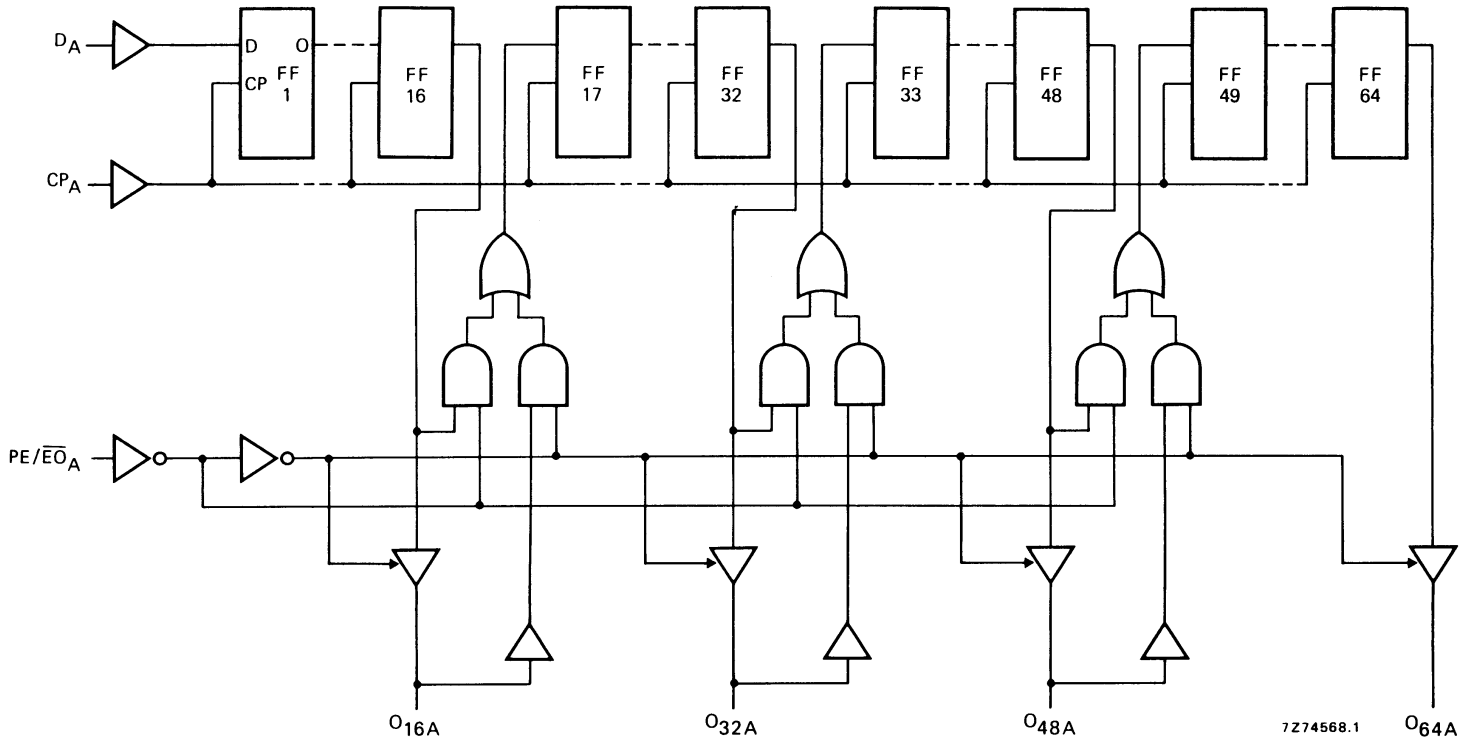






Fig.3 Logic diagram (one shift register).



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FUNCTION TABLE

INPUTS			INPUTS/OUTPUTS				MODE
CP	D	PE/ $\overline{EO}$	O <sub>16</sub>	O <sub>32</sub>	O <sub>48</sub>	O <sub>64</sub>	
	data entered into 1st bit	L	content of 16th bit displayed	content of 32nd bit displayed	content of 48th bit displayed	content of 64th bit displayed	One 64-bit shift register. The content of the shift register is shifted over one stage
	data entered into 1st bit	H	data at O <sub>16</sub> entered into 17th bit	data at O <sub>32</sub> entered into 33rd bit	data at O <sub>48</sub> entered into 49th bit	remains in 'Z' state	Four 16-bit shift register. The content of the shift registers is shifted over one stage.
	X	L	no change	no change	no change	no change	no change
	X	H	Z	Z	Z	Z	no change

## Notes

- H = HIGH state (the more positive voltage)  
L = LOW state (the less positive voltage)  
X = state is immaterial  
Z = high impedance state  
 = positive-going transition  
 = negative-going transition

## Dual 64-bit static shift register

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LSI**AC CHARACTERISTICS** $V_{SS} = 0\text{ V}$ ;  $T_{amb} = 25\text{ }^{\circ}\text{C}$ ; input transition times  $\leq 20\text{ ns}$ 

	$V_{DD}$ V	TYPICAL FORMULA FOR P ( $\mu\text{W}$ )	
Dynamic power dissipation per package (P)	5 10 15	$7\,000 f_i + \sum (f_o C_L) \times V_{DD}^2$ $28\,000 f_i + \sum (f_o C_L) \times V_{DD}^2$ $70\,000 f_i + \sum (f_o C_L) \times V_{DD}^2$	where $f_i$ = input freq. (MHz) $f_o$ = output freq. (MHz) $C_L$ = load capacitance (pF) $\sum (f_o C_L)$ = sum of outputs $V_{DD}$ = supply voltage (V)

**AC CHARACTERISTICS** $V_{SS} = 0\text{ V}$ ;  $T_{amb} = 25\text{ }^{\circ}\text{C}$ ;  $C_L = 50\text{ pF}$ ; input transition times  $\leq 20\text{ ns}$ 

	$V_{DD}$ V	SYMBOL	MIN.	TYP.	MAX.	TYPICAL EXTRAPOLATION FORMULA		
Propagation delays CP $\rightarrow$ O <sub>n</sub> HIGH to LOW	5	$t_{PHL}$		220	440	ns	$193\text{ ns} + (0,55\text{ ns/pF}) C_L$	
	10		85	170	ns	$74\text{ ns} + (0,23\text{ ns/pF}) C_L$		
	15		60	120	ns	$52\text{ ns} + (0,16\text{ ns/pF}) C_L$		
	LOW to HIGH	5	$t_{PLH}$		190	380	ns	$163\text{ ns} + (0,55\text{ ns/pF}) C_L$
		10		75	150	ns	$64\text{ ns} + (0,23\text{ ns/pF}) C_L$	
		15		50	100	ns	$42\text{ ns} + (0,16\text{ ns/pF}) C_L$	
Output transition times HIGH to LOW	5	$t_{THL}$		60	120	ns	$10\text{ ns} + (1,0\text{ ns/pF}) C_L$	
	10		30	60	ns	$9\text{ ns} + (0,42\text{ ns/pF}) C_L$		
	15		20	40	ns	$6\text{ ns} + (0,28\text{ ns/pF}) C_L$		
	LOW to HIGH	5	$t_{TLH}$		60	120	ns	$10\text{ ns} + (1,0\text{ ns/pF}) C_L$
		10		30	60	ns	$9\text{ ns} + (0,42\text{ ns/pF}) C_L$	
		15		20	40	ns	$6\text{ ns} + (0,28\text{ ns/pF}) C_L$	

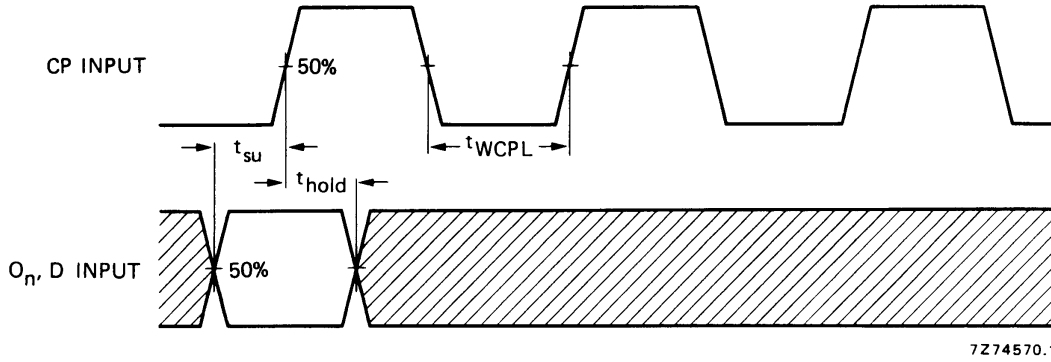
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LSI**AC CHARACTERISTICS** $V_{SS} = 0\text{ V}$ ;  $T_{amb} = 25\text{ }^{\circ}\text{C}$ ;  $C_L = 50\text{ pF}$ ; input transition times  $\leq 20\text{ ns}$ 

	$V_{DD}$ V	SYMBOL	MIN.	TYP.	MAX.			
Minimum clock pulse width; LOW	5	$t_{WCPL}$		95	190	ns	see also waveforms Fig.4.	
	10			40	80	ns		
	15			30	60	ns		
Set-up times $O_n, D \rightarrow CP$	5	$t_{su}$	30	10		ns		
	10		25	5		ns		
	15		20	5		ns		
Hold time $O_n, D \rightarrow CP$	5	$t_{hold}$	45	15		ns		
	10		30	10		ns		
	15		25	10		ns		
3-state propagation delays Output disable times $PE/\overline{EO} \rightarrow O_n$ HIGH  LOW  Output enable times $PE/\overline{EO} \rightarrow O_n$ HIGH  LOW  Maximum clock pulse frequency	5	$t_{PHZ}$		40	80	ns		
			10		30	60		ns
				15		25		50
	5	$t_{PLZ}$				50	100	ns
			10			30	60	ns
				15		25	50	ns
	5	$t_{PZH}$				45	90	ns
			10			25	50	ns
				15		20	40	ns
	5	$t_{PZL}$				60	120	ns
			10			30	60	ns
				15		25	50	ns
5	$f_{max}$	2			5		MHz	
		10	6		12		MHz	
			15	8	16		MHz	

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Fig.4 Waveforms showing minimum clock pulse width, set-up and hold times for O<sub>n</sub> (as data input) and D to CP.